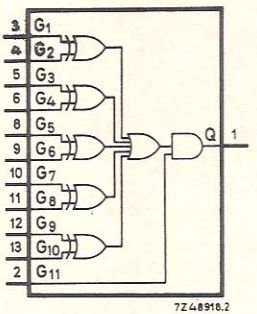
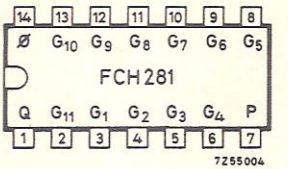
The FC family of DTL silicon monolithic integrated circuits has been designed for medium speed digital applications in computing, office electronics, telecommunication, instrumentation and industrial control.

development sample data

SINGLE 5-BIT COMPARATOR





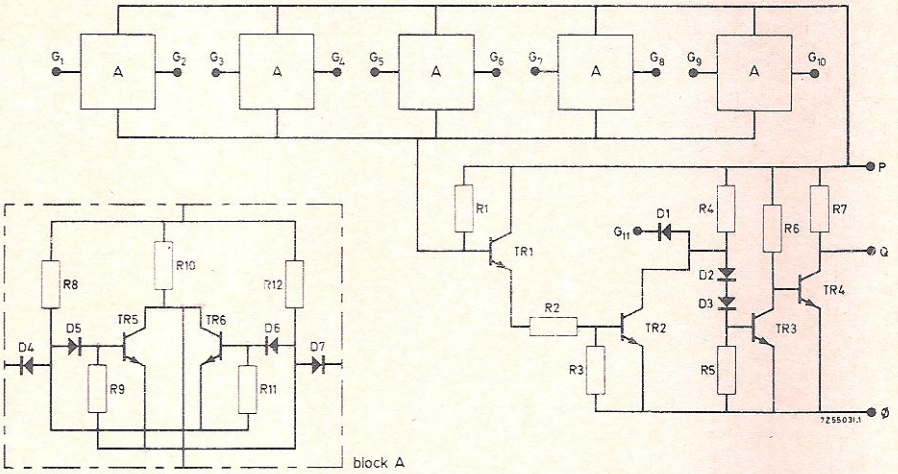
Package XG14; dual in-line

QUICK REFERENCE DATA			
Supply voltage	V_P	6.0 ± 5%	V
Operating ambient temperature range	T_{amb}	0 to +75	°C
Average propagation delay time N = 6, C_W = 60 pF, T_{amb} = 25 °C	t_{pd}	typ. 150	ns
Available d.c. fan-out T_{amb} = 0 to +75 °C	N_a	⩾ 7	
D.C. noise margin T_{amb} = 25 °C	M_L	typ. 1.2	V
Power consumption 50% duty cycle, T_{amb} = 25 °C	P_{av}	typ. 50	mW

The FCH281 comprises five exclusive-OR functions followed by inverter stages, an OR gate, and an AND gate. If on one or more pairs (G_1-G_2, --- G_9-G_{10}) one input is LOW and the other HIGH then the output will be HIGH provided G_{11} is HIGH. Otherwise the output will be LOW.

These data, based on the specifications and measured performance of development samples, afford a preliminary indication of the characteristics to be expected of the described product. Distribution of development samples implies no guarantee as to the subsequent availability of the product

CIRCUIT DIAGRAM



FUNCTION TABLE

$G_1\,G_2$	$G_3\,G_4$	$G_5\,G_6$	$G_7\,G_8$	$G_9\,G_{10}$	G_{11}	Q
Equal	Equal	Equal	Equal	Equal	H	L
Unequal	X	X	X	X	H	H
X	Unequal	X	X	X	H	H
X	X	Unequal	X	X	H	H
X	X	X	Unequal	X	H	H
X	X	X	X	Unequal	H	H
X	X	X	X	X	L	L

G_1	G_2	
L	L	Equal
L	H	Unequal
H	L	Unequal
H	H	Equal

H = HIGH state (the more positive voltage)
L = LOW state (the less positive voltage)
X = state is immaterial

LOGIC FUNCTION (continued)

$$Q = \Big[\overline{(\overline{G}_1 \cdot \overline{G}_2 + G_1 \cdot G_2)} + \overline{(\overline{G}_3 \cdot \overline{G}_4 + G_3 \cdot G_4)} + \overline{(\overline{G}_5 \cdot \overline{G}_6 + G_5 \cdot G_6)} + \overline{(\overline{G}_7 \cdot \overline{G}_8 + G_7 \cdot G_8)} + \overline{(\overline{G}_9 \cdot \overline{G}_{10} + G_9 \cdot G_{10})}\Big] \cdot G_{11}.$$

RATINGS Limiting values in accordance with the Absolute Maximum System (IEC134)

Supply voltage	V_P	max.	8.0	V
Output voltage	V_Q	max.	8.0	V
Input voltage	V_G	max.	8.0	V
Output current [1]	$-I_Q$	max.	20	mA
Input current [2]	$-I_G$	max.	20	mA
Voltage difference between any two inputs		max.	8.0	V
Storage temperature	T_{stg}	−55 to	+125	°C
Operating ambient temperature	T_{amb}	0 to	+75	°C

1) For negative output voltage.
2) At this limit input voltage typ. : −1.5 V.

SYSTEM DESIGN DATA

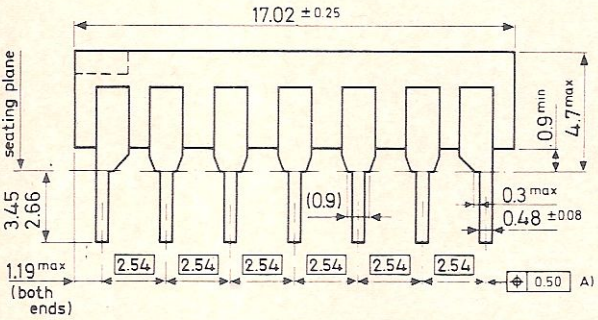
Uniform system temperature	T_{amb}	0 to +75		°C
Uniform system supply voltage	V_P	5.7 to 6.3		V
Available d.c. fan out	N_a	⩾	7	
D.C. noise margin	M_L	min.	0.4	V
	M_H	min.	1.5	V
Average propagation delay time	t_{pd}	max.	250	ns
Equivalent input capacitance	C_G	typ.	4	pF
Supply current (duty cycle 50%)	I_{Pav}	typ.	10	mA
Power dissipation at T_{amb} = 75 °C	P_{tot}	max.	90	mW

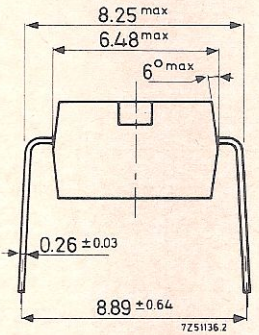
CHARACTERISTICS

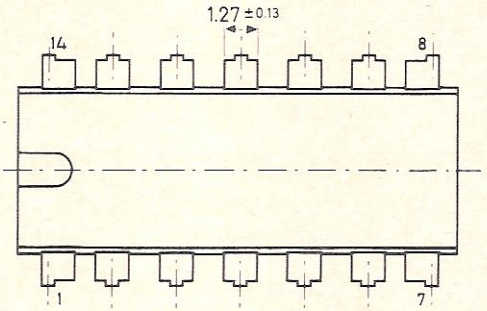
		T_{amb} (°C)				Conditions and references	
		0	+25	+75		V_P (V)	
STATIC DATA							
Output voltage LOW	V_{QLmax}	0.4	0.4	0.4	V	5.7 and 6.3	For the proper combination of inputs to be HIGH or LOW see Function Table
at: Output current LOW	I_{QLmax}	14.0	14.0	14.0	mA	5.7	
		14.0	14.0	14.0	mA	6.3	
Output voltage HIGH	V_{QHmin}	5.3	5.3	5.3	V	5.7 and 6.3	$I_Q = 0$
	V_{QHmin}	4.7	4.7	4.5	V	5.7	$I_Q = -200\ \mu A$
at: Input voltage LOW	V_{GLmax}	1.0	1.0	0.8	V	5.7 and 6.3	For the proper combination of inputs to be HIGH or LOW see Function Table
and at: Input voltage HIGH	V_{GHmin}	3.0	2.8	2.5	V	5.7 and 6.3	
Input current LOW	$-I_{G1\ to\ 10\ Lmax}$	1.75	1.65	1.55	mA	5.7	$V_{G1\ to\ 10} = 0.4$ V
	$-I_{G1\ to\ 10\ Lmax}$	2.0	1.9	1.8	mA	6.3	$V_{G1\ to\ 10} = 0.4$ V
	$-I_{G11\ Lmax}$	1.2	1.1	1.05	mA	5.7	$V_{G11} = 0.4$ V
	$-I_{G11\ Lmax}$	1.35	1.25	1.20	mA	6.3	$V_{G11} = 0.4$ V
Input current HIGH	I_{GHmax}	1.0	1.0	25	μA	5.7	$V_G = 5.3$ V other inputs 0 V
Supply current	I_{Pmax}	15.3	14.5	13.0	mA	6.3	G inputs LOW

PACKAGE OUTLINE
XG14; dual in-line

Dimensions in mm







A) The spacing between centerlines of any two pins is equal to the true position spacing of 2.54 mm per pin with a total tolerance of ± 0.25 mm.

Handling notes

1. Devices may be soldered directly into circuits with soldering irons. At iron temperatures below 245 °C the maximum soldering time should be less than 10 seconds and at iron temperatures between 245 °C and 400 °C the soldering time should be less than 5 seconds. In both cases the soldering iron should be applied below the seating plane (see outline drawing).

2. Devices mounted up to the seating plane on a printed circuit board may be dip or flow soldered providing the solder temperature is below 245 °C and the time of immersion is less than 5 seconds. The body temperature should not be allowed to exceed the maximum storage temperature during soldering. If excessive preheat cycles are used, it may be necessary to cool the printed board immediately after leaving the solder bath/wave in order that this requirement is met.